AMENDMENTS TO CLAIMS

Claim 1 (original): A method for adding an additional layer to an integrated circuit, the method comprising:

providing an integrated circuit having an interconnect layer;

depositing, over substantially all of an exposed surface of the integrated circuit, an additional layer of material whose conductivity can be altered; and

selectively altering the conductivity of a first portion of the additional layer by selective annealing, to produce a sub-circuit in the additional layer, the sub-circuit being in operative electrical communication with the integrated circuit.

Claim 2 (original): The method according to claim 1 and wherein the selective annealing comprises selective laser annealing.

Claim 3 (currently amended): The method according to claim 1 ~~or claim 2~~ and wherein the sub-circuit is not visually distinguishable from a second portion of the additional layer, the second portion being disjoint from the first portion.

Claim 4 (original): The method according to claim 3 and wherein the second portion comprises substantially all parts of the additional layer not comprised in the first portion.

Claim 5 (currently amended): The method according to claim 1 ~~any of claims~~ [[1 - 4]] and wherein the selectively altering comprises altering substantially without removing any part of the additional layer.

Claim 6 (currently amended): An integrated circuit produced by the method of claim 1 ~~any of claims 1 – 5~~.

Claim 7 (original): A method for adding an additional layer to a plurality of integrated circuits, the method comprising:

providing a plurality of integrated circuits, each having an interconnect layer;

performing the following for each one of the plurality of integrated circuits:

depositing, over substantially all of an exposed surface of the one integrated circuit, an additional layer of material whose conductivity can be altered; and

selectively altering the conductivity of a first portion of the additional layer by selective annealing, to produce a sub-circuit in the additional layer, the sub-circuit being in operative electrical communication with the integrated circuit,

wherein the first portion of each integrated circuit has a shape, and, for at least a first integrated circuit and a second integrated circuit of the plurality of integrated circuits, the shape of the first portion of the first integrated circuit is different from the shape of the first portion of the second integrated circuit.

Claim 8 (original): The method according to claim 7 and wherein the shape of the first portion of each one of the plurality of integrated circuits on a production wafer is different from the shape of the first portion of any other of the plurality of integrated circuits on the production wafer.

Claim 9 (currently amended): The method according to ~~either~~ claim 7 ~~or claim 8~~ and wherein the selective annealing comprises selective laser annealing.

Claim 10 (currently amended): The method according to claim 7 ~~any of claims 7-9~~ and wherein the sub-circuit is not visually distinguishable from a second portion of the additional layer, the second portion being disjoint from the first portion.

Claim 11 (original): The method according to claim 10 and wherein the second portion comprises substantially all parts of the additional layer not comprised in the first portion.

Claim 12 (currently amended): The method according to claim 7 ~~any of claims 7-11~~ and wherein the selectively altering comprises altering substantially without removing any part of the additional layer.

Claim 13 (currently amended): A plurality of integrated circuits, produced by the method of claim 7 ~~any of claims 7-12~~.

Claim 14 (original): A method for adding an additional layer to an integrated circuit, the method comprising:

providing an integrated circuit having an interconnect layer;

depositing, over substantially all of an exposed surface of the integrated circuit, an additional layer of material whose conductivity can be altered;

selectively doping only a first portion of the additional layer of material; and

selectively altering the conductivity of the first portion of the additional layer by annealing, to produce a sub-circuit in the additional layer, the sub-circuit being in operative electrical communication with the integrated circuit.

Claim 15 (original): The method according to claim 14 and wherein the sub-circuit is not visually distinguishable from a second portion of the additional layer, the second portion being disjoint from the first portion.

Claim 16 (original): The method according to claim 15 and wherein the second portion comprises substantially all parts of the additional layer not comprised in the first portion.

Claim 17 (currently amended): An integrated circuit produced by the method of claim 14 ~~any of claims 14 - 16~~.

Claim 18 (original): A method for adding an additional layer to a plurality of integrated circuits, the method comprising:

providing a plurality of integrated circuits, each having an interconnect layer;

depositing, over substantially all of an exposed surface of each of the plurality of integrated circuits, an additional layer of material whose conductivity can be altered;

for each one of the plurality of integrated circuits, selectively doping only a first portion of the additional layer of material of the one integrated circuit; and

selectively altering the conductivity of the first portion of the additional layer of each of the plurality of integrated circuits by annealing, to produce a sub-circuit in the additional layer, the sub-circuit being in operative electrical communication with the integrated circuit,

wherein the first portion of each integrated circuit has a shape, and, for at least a first integrated circuit and a second integrated circuit of the plurality of integrated circuits, the shape of the first portion of the first integrated circuit is different from the shape of the first portion of the second integrated circuit.

Claim 19 (original): The method according to claim 18 and wherein the shape of the first portion of each one of the plurality of integrated circuits on a production wafer is different from the shape of the first portion of any other of the plurality of integrated circuits on the production wafer.

Claim 20 (currently amended): The method according to claim 18 ~~or claim 19~~ and wherein the sub-circuit is not visually distinguishable from a second portion of the additional layer, the second portion being disjoint from the first portion.

Claim 21 (original): The method according to claim 20 and wherein the second portion comprises substantially all parts of the additional layer not comprised in the first portion.

Claim 22 (currently amended): A plurality of integrated circuits, produced by the method of claim 18 ~~any of claims 18 - 21~~.

Claim 23 (original): An integrated circuit comprising:

a lower integrated circuit portion including an interconnect layer; and

an additional layer of material disposed over substantially all of a surface of the lower integrated circuit portion, the additional layer comprising a first portion, the first portion comprising a sub-circuit in operative electrical communication with the lower integrated circuit portion, the sub-circuit being not visually distinguishable from a second portion of the additional layer, the second portion being disjoint from the first portion.

Claim 24 (original): The integrated circuit according to claim 23 wherein the second portion comprises substantially all parts of the additional layer not comprised in the first portion.

Claim 25 (new): A method for producing an integrated circuit, the method comprising:

providing a lower integrated circuit portion including an interconnect layer; and

producing an additional layer of material disposed over substantially all of a surface of the lower integrated circuit portion, the additional layer comprising a first portion, the first portion comprising a sub-circuit in operative electrical communication with the lower integrated circuit portion, the sub-circuit being not visually distinguishable from a second portion of the additional layer, the second portion being disjoint from the first portion.

Claim 26 (new): The method according to claim 25 and wherein the producing comprises:

depositing, over substantially all of an exposed surface of the lower integrated circuit portion, an additional layer of material whose conductivity can be altered; and

selectively altering the conductivity of a first portion of the additional layer by selective annealing, thereby producing the sub-circuit.

Claim 27 (new): The method according to claim 26 and wherein the selective annealing comprises selective laser annealing.

Claim 28 (new): The method according to claim 26 and wherein the selectively altering comprises altering substantially without removing any part of the additional layer.

Claim 29 (new): The method according to claim 25 and wherein the producing comprises:

depositing, over substantially all of an exposed surface of the lower integrated circuit portion, an additional layer of material whose conductivity can be altered;

selectively doping only a first portion of the additional layer of material; and

selectively altering the conductivity of the first portion of the additional layer by annealing.

Claim 30 (new): The method according to claim 25 and wherein the second portion comprises substantially all parts of the additional layer not comprised in the first portion.

Claim 31 (new): The method according to claim 25 and wherein the first portion has a shape, and, for at least a first integrated circuit and a second integrated circuit of a plurality of integrated circuits on a production wafer, the shape of the

first portion of the first integrated circuit is different from the shape of the first portion of the second integrated circuit.

Claim 32 (new): The method according to claim 31 and wherein the shape of the first portion of each one of the plurality of integrated circuits on a production wafer is different from the shape of the first portion of any other of the plurality of integrated circuits on a production wafer.